**Half adder using Verilog HDL Programming**

# **Program:**

module ha(a,b,sample,carry);

input a,b;

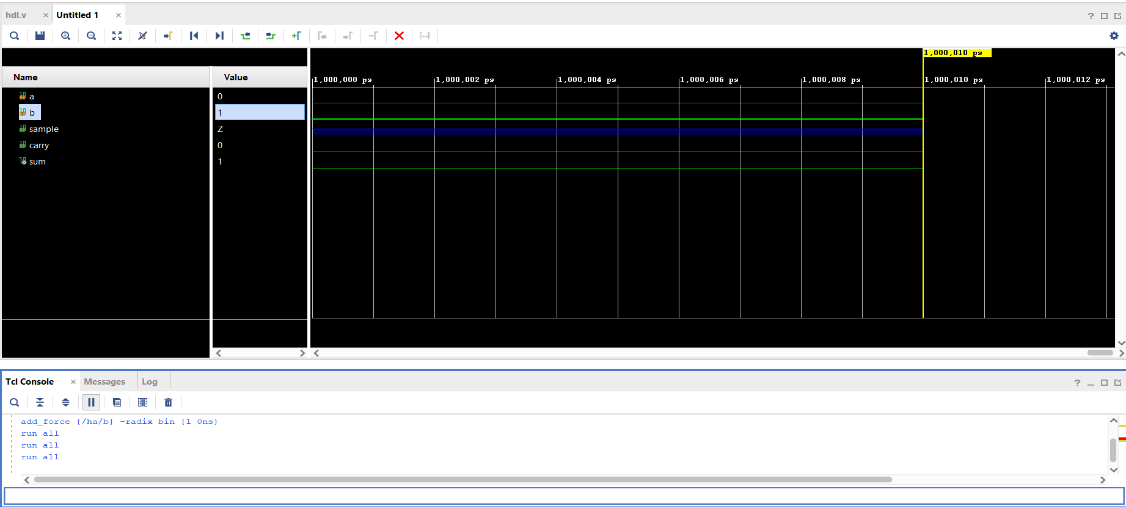
output sample,carry;

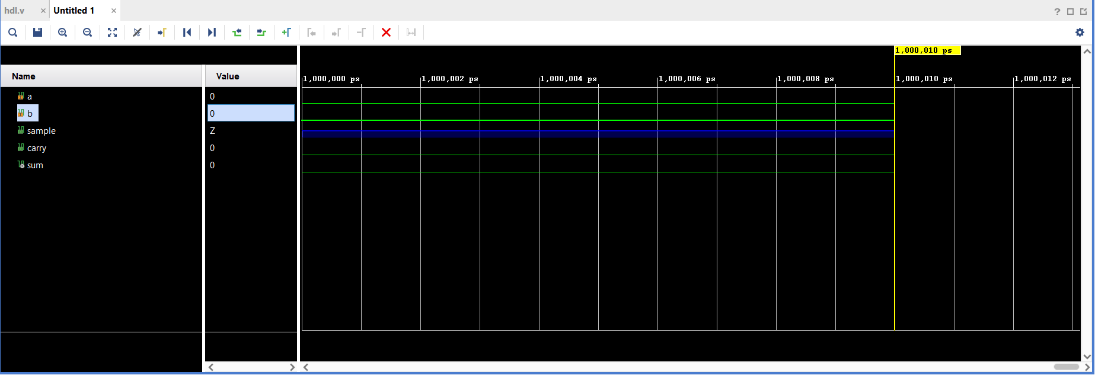
assign sum=a^b;

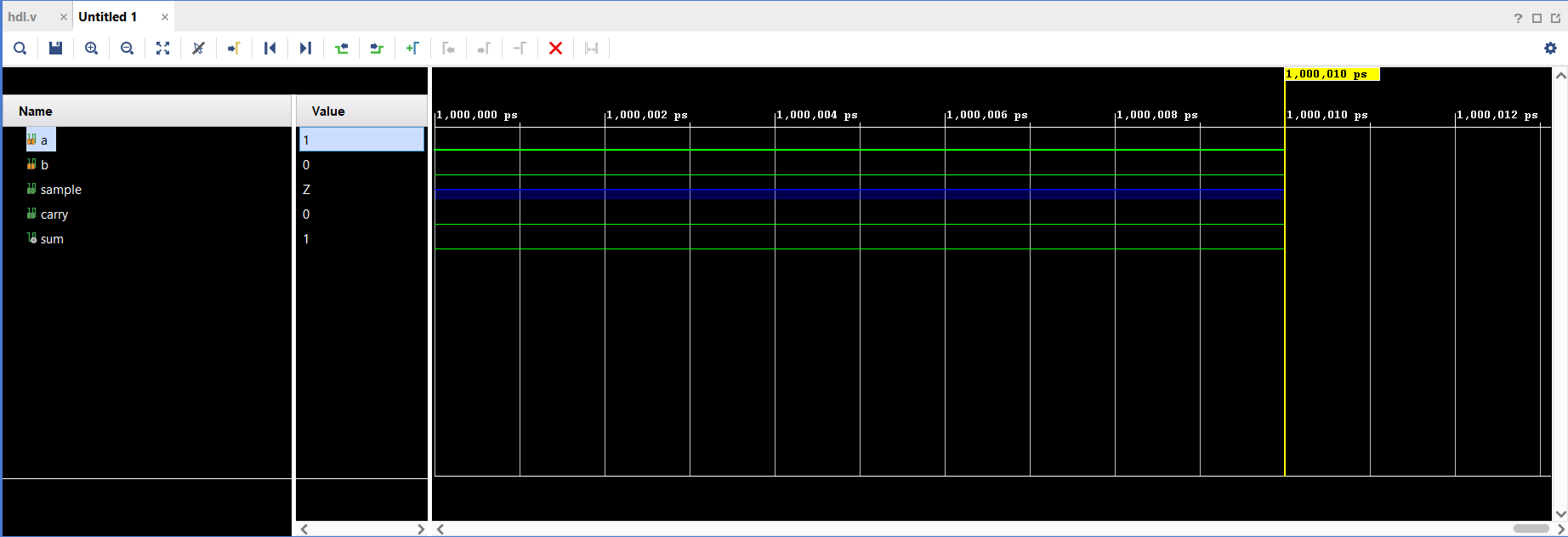
assign carry=a&b;

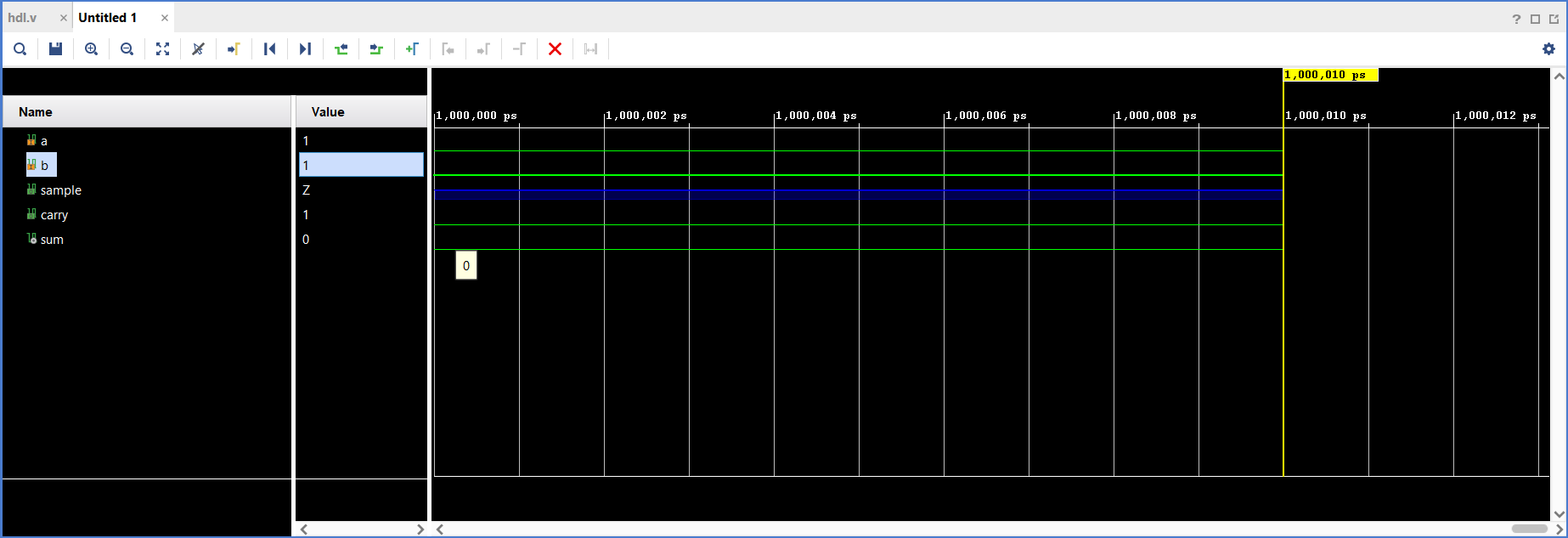
endmodule

**Output:**

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